Program : **B.Tech**

Subject Name: **Computer System Organisation**

Subject Code: **EC-504**

Semester: **5th**

Unit II

Control Unit Organization

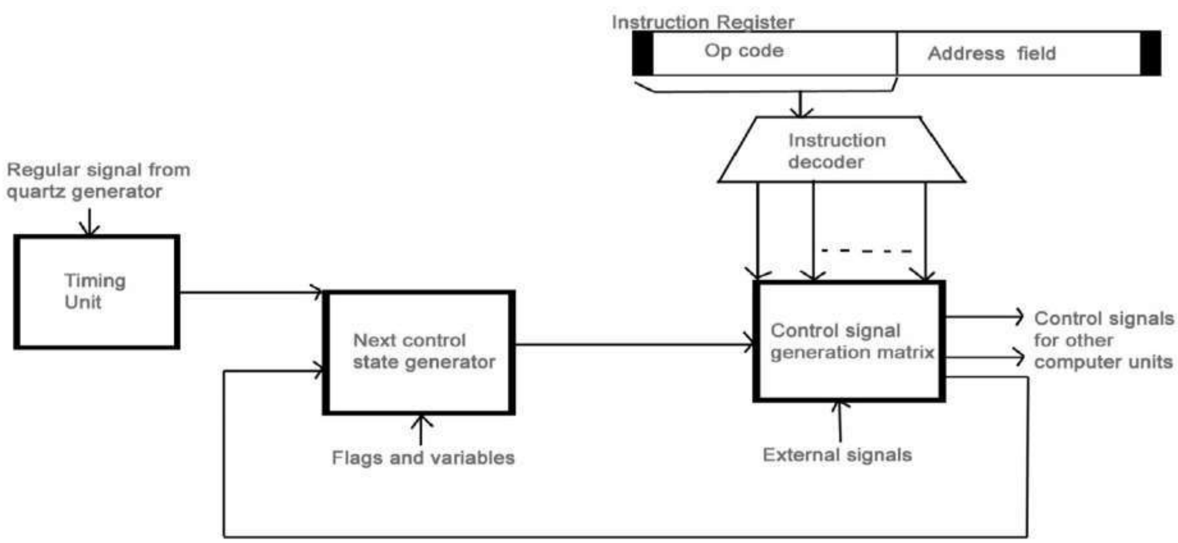
2.1 Hardwired Control Unit

The control hardware can be viewed as a state machine that changes from one state to another in every clock cycle, depending on the contents of the instruction register, the condition codes and the external inputs. The outputs of the state machine are the control signals. The sequence of the operation carried out by this machine is determined by the wiring of the logic elements and hence named as "hardwired".

- Fixed logic circuits that correspond directly to the Boolean expressions are used to generate the control signals.

- Hardwired control is faster than micro-programmed control.

- A controller that uses this approach can operate at high speed.

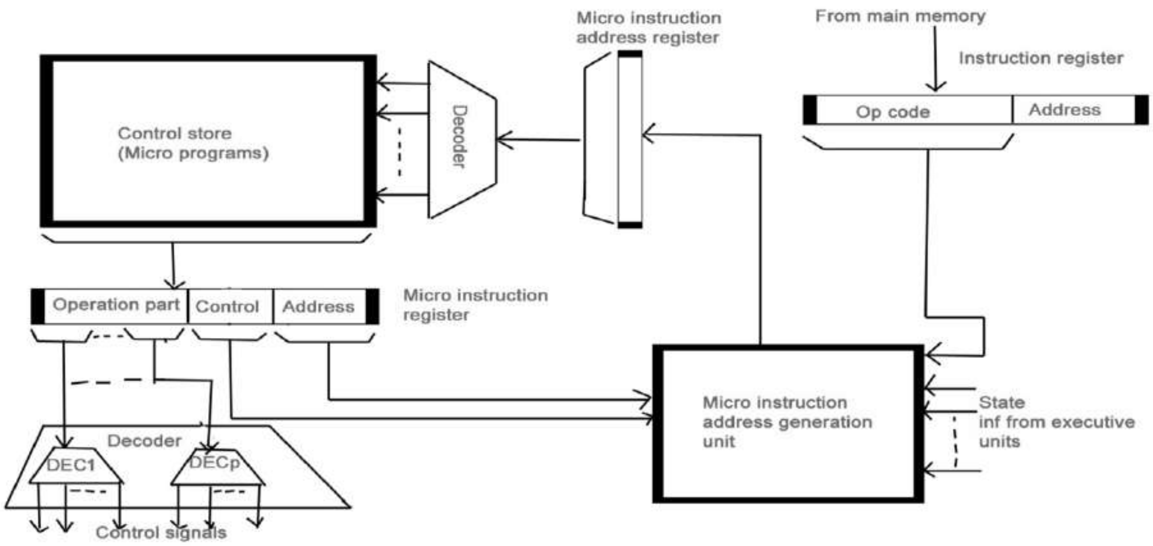


2.2 Micro-programmed Control Unit

- The control signals associated with operations are stored in special memory units inaccessible by the programmer as Control Words.
- Control signals are generated by a program are similar to machine language programs.
- Micro-programmed control unit is slower in speed because of the time it takes to fetch microinstructions from the control memory.

Some Important Terms –

1. Control Word: A control word is a word whose individual bits represent various control signals.
2. Micro-routine: A sequence of control words corresponding to the control sequence of a machine instruction constitutes the micro-routine for that instruction.
3. Micro-instruction: Individual control words in this micro-routine are referred to as microinstructions.
4. Micro-program: A sequence of micro-instructions is called a micro-program, which is stored in a ROM or RAM called a Control Memory (CM).
5. Control Store : the micro-routines for all instructions in the instruction set of a computer are stored in a special memory called the Control Store



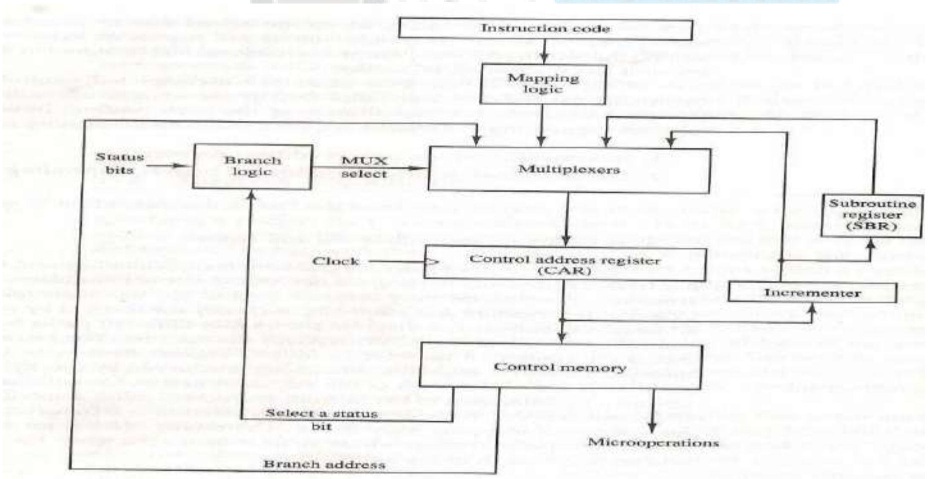
2.3 Address Sequencing

Micro instructions are stored in the control memory in groups called as a Routine. The hardware which controls the address sequencing should also be capable of sequencing the microinstructions within a routine and be able to branch from one routine to another. To understand the address sequencing in a microprogram control unit, let us evaluate the steps that the control unit must undergo during the execution of a single computer instruction.

After an Instruction is fetched it has to be mapped, such that the mapping will give the address location where the instruction is present in the control memory. In brief the address sequencing capabilities required in a control memory are:

- Incrementing of the Control address Register
- Unconditional branching or conditional branching depending on the status bit conditions.
- A mapping process from the bits of the instruction to an address of control memory.
- A facility for subroutine call and return.

The following figure explains the above steps:



2.4 Micro Instruction Format

The microinstruction format for the control memory is shown in the figure. The 20 bits of the microinstruction are divided into four functional parts as follows:

1.The three fields F1, F2, and F3 specify micro operations for the computer. The micro operations subdivided into three fields of three bits each. The three bits in each field are encoded to specify seven distinct micro operations. So, this gives a total of 21 micro operations.

2.Also, The CD field selects status bit conditions.

3.Moreover, The BR field specifies the type of branch to use.

4.The AD field contains a branch address. The address field is seven bits wide since the control memory has $128 = 2^7$ words.

3	3	3	2	2	7
F1	F2	F3	CD	BR	AD

F1, F2, F3: Microoperation fields
CD: Condition for branching
BR: Branch field
AD: Address field

Figure: Microinstruction Format

As an example, a microinstruction can specify two simultaneous micro operations between F2 and F3 and none from F1.

DR ←M[AR] with F2 = 100

PC ← PC + 1 with F3 = 101

The nine bits of the micro operation fields will then be 000 100 101.

The CD (condition) field consists of two bits which encoded to specify four status bit conditions as listed in Table.

CD	Condition	Symbol	Comments
00	Always = 1	U	Unconditional branch
01	DR(15)	I	Indirect address bit
10	AC(15)	S	Sign bit of AC
11	AC = 0	Z	Zero value in AC

Table: Condition Field

The BR (branch) field consists of two bits. It used, in conjunction with the address field AD, to choose the address of the next microinstruction shown in Table.

BR	Symbol	Function
00	JMP	CAR ← AD if condition = 1 CAR ← CAR + 1 if condition = 0
01	CALL	CAR ← AD, SBR ← CAR + 1 if condition = 1 CAR ← CAR + 1 if condition = 0
10	RET	CAR ← SBR (Return from subroutine)
11	MAP	CAR(2-5) ← DR(11-14), CAR(0,1,6) ← 0

2.5 Microprogram Sequencer

- The basic components of a microprogrammed control unit are the control memory and the circuits that select the next address.
- Also, The address selection part is called a microprogram sequencer.
- A microprogram sequencer can be constructed with digital functions to suit a particular application.
- Moreover, To guarantee a wide range of acceptability, an integrated circuit sequencer must provide an internal organization that can adapt to a wide range of applications.
- The purpose of a microprogram sequencer is to present an address to the control memory so that a microinstruction may read and executed.
- Commercial sequencers include within the unit an internal register stack used for temporary storage of addresses during microprogram looping and subroutine calls.
- Some sequencers provide an output register which can function as the address register for the control memory.
- Also, The block diagram of the microprogram sequencer shown in figure 4.6.
- There are two multiplexers in the circuit.
- So, The first multiplexer selects an address from one of four sources and routes it into a control address register CAR.
- The second multiplexer tests the value of a selected status bit and the result of the test applied to an input logic circuit.
- Moreover, The output from CAR provides the address for the control memory.
- The content of CAR incremented and applied to one of the multiplexer inputs and to the subroutine registers SBR.

- Also, The other three inputs to multiplexer 1 come from the address field of the present microinstruction, from the output of SBR, and from an external source that maps the instruction.
- Although the figure shows a single subroutine register, a typical sequencer will have a register stack about four to eight levels deep. In this way, a number of subroutines can be active at the same time.
- The CD (condition) field of the microinstruction selects one of the status bits in the second multiplexer.
- If the bit selected is equal to 1, the T (test) variable is equal to 1; otherwise, it is equal to
- Moreover, The T value together with the two bits from the BR (branch) field goes to an input logic circuit.
- The input logic in a particular sequence will determine the type of operations that are available in the unit.

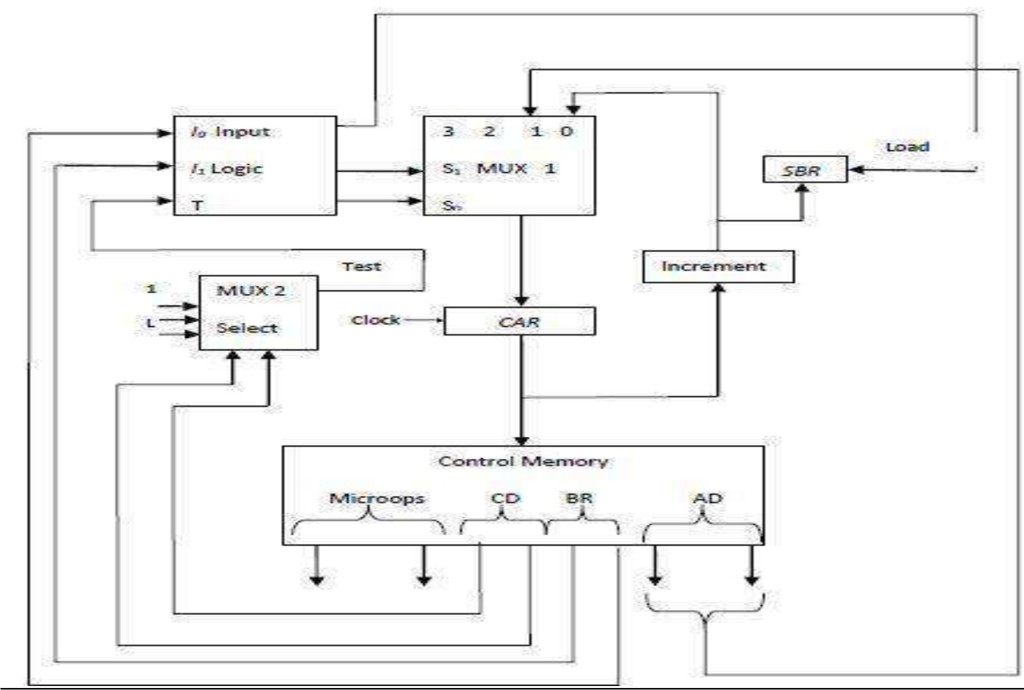


Figure: Microprogram Sequencer for a control memory

